Section 6:

Macro Library

Q14000 BICOMS

6-1-1 Q14000 TTL MACROS

- FOR ANY TTL INPUT/OUTPUT IN A SINGLE +5V POWER SUPPLY CIRCUIT

	MACRONAME	OPTION	TYPE	SIZE	DESCRIPTION
6-1-3	IT12	S,H	IO	1	TTL INPUT
6-1-4	OT21	S,H	IO	1	TTL OUTPUT WITH NOR
6-1-5	OT24	S,H	IO	1	TTL 3-STATED OUTPUT
6-1-6	UT27	S,H	IO	1	TTL BIDIRECTIONAL I/O

6-2-1 Q14000 TTLMIX MACROS

- FOR TTL INPUT/OUTPUT IN ECL/TTL MIXED CIRCUIT WITH TWO POWER SUPPLIES (-5.2V AND +5V FOR ECL 10K INPUT, ANY ECL OUTPUT OR -4.5V AND +5V FOR ECL 100K INPUT, ANY ECL OUTPUT).

	MACRONAME	OPTION	TYPE	SIZE	DESCRIPTION
6-2-3	IT52	S	IO	1	TTLMIX INPUT
6-2-4	OT61	S	IO	1	TTLMIX OUTPUT WITH OR
6-2-5	OT64	S	IO	1	TTLMIX 3-STATED OUTPUT
6-2-6	UT67	S	IO	1	TTLMIX BIDIRECTIONAL I/O

6-3 Q14000 ECL MACROS

- FOR ECL INPUT/OUTPUT IN ANY CIRCUIT, +5V ECL, STD ECL, AND ECL/TTL MIX CIRCUITS

```
     OEnn IS USED FOR ECL 10K
     OKnn IS USED FOR ECL 100K
     UEnn IS USED FOR BIDIRECTIONAL ECL 10K
     UKnn IS USED FOR BIDIRECTIONAL ECL 100K
```

	MACRONAME	OPTION	TYPE	SIZE	DESCRIPTION
6-3-3	IE23	S,H	IO	1	ECL INPUT
6-3-4	Ox70	S	IO	1	ECL OUTPUT WITH OR
6-3-5	UE49	S,H	IO	1	ECL BIDIRECTIONAL I/O

6-4-1 Q14000 INTERNAL LOGIC MACROS
• S-OPTION ONLY - NO OTHER OPTIONS AVAILABLE

EXOR/EXNOR GATES

	MACRONAME	TYPE	SIZE	DESCRIPTION
6-4-3	EX02	BASIC	1	EXCLUSIVE OR
6-4-4	EX04	BASIC	1	2-INPUT XNOR

FLIP/FLOPS

	MACRONAME	TYPE	SIZE	DESCRIPTION
6-4-5	FF01	BASIC	2	D F/F
6-4-6	FF02	BASIC	2	D F/F WITH AR
6-4-7	FF03	BASIC	2	D F/F WITH AS
6-4-8	FF04	BASIC	2	D-FF W/AS-AR
6-4-9	FF11	BASIC	3	D F/F
6-4-10	FF12	BASIC	3	SET-SCAN D F/F WITH 2:1 MUX; AR
6-4-12	FF13	BASIC	3	SET-SCAN D F/F WITH 2:1 MUX; AS
6-4-14	FF14	BASIC	3	SET SCAN D F/F W/2:1 MUX; AR;AS
6-4-15	FF23	BASIC	3	JK F/F WITH AR
6-4-16	FF24	BASIC	3	J-K FLIP-FLOP WITH AR; AS

6-6-1 SPECIAL MACROS

	MACRONAME	CELL	SIZE	DESCRIPTION
6-6-3	ITPWR	I/O	1	ADDED VCC PIN FOR TTL
6-6-3	ITGND	I/O	1	ADDED GROUND PIN FOR TTL
6-6-4	IEVCC	I/O	1	ADDED ECL VCC SUPPLY

CHIPMACROS - USE NO CELLS; MUST USE 1 PER CIRCUIT

6-6-6	Q9100BTTL	FOR 100% TTL; Q9100B ARRAY
6-6-7	Q9100BECL10K	FOR 100% ECL10K; Q9100B ARRAY
6-6-7	Q9100BECL100K	FOR 100% ECL100K; Q9100B ARRAY
6-6-8	Q9100BMIX10K	DUAL SUPPLY ECL100K/TTL; Q9100B ARRAY
6-6-8	Q9100BMIX100K	DUAL SUPPLY ECL100K/TTL; Q9100B ARRAY
6-6-9	Q9100BTTL10K	FOR +5V ECL10K/TTL; Q9100B ARRAY
6-6-9	Q9100BTTL100K	FOR +5V ECL100K/TTL; Q9100B ARRAY
6-6-6	Q2100BTTL	FOR 100% TTL; Q2100B ARRAY
6-6-7	Q2100BECL10K	FOR 100% ECL10K; Q2100B ARRAY
6-6-7	Q2100BECL100K	FOR 100% ECL100K; Q2100B ARRAY
6-6-8	Q2100BMIX10K	DUAL SUPPLY ECL100K/TTL; Q2100B ARRAY
6-6-8	Q2100BMIX100K	DUAL SUPPLY ECL100K/TTL; Q2100B ARRAY
6-6-9	Q2100BTTL10K	FOR +5V ECL10K/TTL; Q2100B ARRAY
6-6-9	Q2100BTTL100K	FOR +5V ECL100K/TTL; Q2100B ARRAY

MACRO NAMING CONVENTION- Q14000

THE EXPANSION OF A MACRO NAME IS GIVEN BELOW:

```
aa[a]nnb
 :   : :
 :   : :
 :   : :
 :   : :
 :   : :
 :   : :
 :   : ---- POWER/FAN-OUT  S - STANDARD      (30 LOADS)
 :   :                        high-fan-out  (50 LOADS)
 :   :                     H - HIGH SPEED    (30 LOADS)
 :   :                     (3-STATE DRIVERS - 8 LOADS)
 :   :
 :   --------- CELL # (00-119)
 --------- CELL TYPE: TWO - THREE LETTERS
                      (THREE LETTERS FOR MSI MACROS)
```

KEY:

AD - ADDER
ADD - MSI ADDER
BB - MSI BUILDING BLOCK - AMCC USE ONLY
BI - ECL INPUT BUFFERED LOGIC
CPG - MSI CARRY LOOK-AHEAD GENERATOR
CMP - MSI COMPARATOR
CTR - MSI COUNTER
DE - DECODER
DEC - MSI DECODER
EX - EXOR
FF - F/F
FFF - MSI F/F
GT - GENERAL GATES
LA - LATCH
MX - MULTIPLEXOR, MUX
REG - MSI REGISTER

IE	ECL input
OE	ECL 10K OUTPUT
UE	ECL 10K Bidirec.
IT	TTL input
OT	TTL output
UT	TTL Bidirectional

FOR TTL I/O MACROS:
00-39 = 100% TTL; OR MIX IN A +5V ONLY CIRCUIT
40-79 = MIX IN A DUAL POWER SUPPLY CIRCUIT

FOR ECL I/O MACROS:
LETTER DESIGNATION FOR ECL 10K AND ECL 100K
ECL MACROS DO NOT VARY WITH I/O MODE

CHIP MACRO NAMING CONVENTION:

Qaaaaabcccdddd

WHERE:

aaaaa 3-5 CHARACTERS THE IDENTIFY THE ARRAY BY NAME:
9100
2100

b CHARACTER THAT DESIGNATES THE FAMILY
B

ccc 3 CHARACTERS THAT IDENTIFY THE I/O MODE
TTL
ECL
MIX FOR TWO-POWER SUPPLIES

dddd 3-4 CHARACTERS TO IDENTIFY THE ECL INPUT TYPE
ØØØ FOR NONE
10K
100K

Section 6-1:

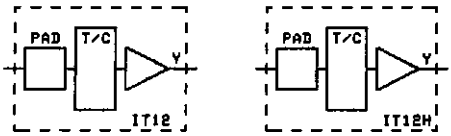
TTL Interface

AMCC Q14000 MACRO SUMMARY - TTL LIB (803)

FOR 100% TTL OR ECL/TTL MIXED MODE CIRCUITS;
SINGLE +5V POWER SUPPLY
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

IT12 1 I/O cell	TTL INPUT			
	S	L	H	
Tpd PAD->Y++	1.96		1.79	ns
--	5.71		5.47	ns
ICC	3.00		3.50	mA I/O
FAN-OUT LOAD LIMIT:	50		50	loads
k FACTOR RISING	0.025		0.025	ns/LU
FALLING	0.030		0.030	ns/LU

Y = PAD



BUFFERED INPUT

6-4-1 Q14000 INTERNAL LOGIC MACROS
• S-OPTION ONLY - NO OTHER OPTIONS AVAILABLE

EXOR/EXNOR GATES

	MACRONAME	TYPE	SIZE	DESCRIPTION
6-4-3	EX02	BASIC	1	EXCLUSIVE OR
6-4-4	EX04	BASIC	1	2-INPUT XNOR

FLIP/FLOPS

	MACRONAME	TYPE	SIZE	DESCRIPTION
6-4-5	FF01	BASIC	2	D F/F
6-4-6	FF02	BASIC	2	D F/F WITH AR
6-4-7	FF03	BASIC	2	D F/F WITH AS
6-4-8	FF04	BASIC	2	D-FF W/AS-AR
6-4-9	FF11	BASIC	3	D F/F
6-4-10	FF12	BASIC	3	SET-SCAN D F/F WITH 2:1 MUX; AR
6-4-12	FF13	BASIC	3	SET-SCAN D F/F WITH 2:1 MUX; AS
6-4-14	FF14	BASIC	3	SET SCAN D F/F W/2:1 MUX; AR;AS
6-4-15	FF23	BASIC	3	JK F/F WITH AR
6-4-16	FF24	BASIC	3	J-K FLIP-FLOP WITH AR; AS

AMCC Q14000 MACRO SUMMARY - TTL LIB (803)

FOR 100% TTL OR ECL/TTL MIXED MODE CIRCUITS;
SINGLE +5V POWER SUPPLY
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OT24 1 I/O cell TTL 3-STATE INVERTING OUTPUT

		S	L	H	
Tpd A->PAD	+-	3.33		2.77	ns
	-+	4.65		3.46	ns
EN->PAD	LZ	2.30		2.30	ns
	HZ	2.30		2.20	ns
	ZL	4.10		4.40	ns
	ZH	3.10		1.00	ns
ICC	ENABLED	2.10		3.40	mA I/O
	DISABLED	3.40		4.70	mA I/O

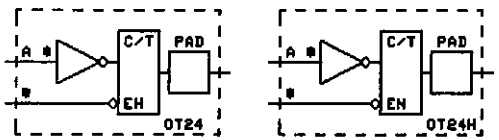
---

* A, EN COUNT AS 3 LOADS EACH

EN	A	PAD
0	0	1
0	1	0
1	0	3-STATE
1	1	3-STATE

EN = 0: PAD = $\bar{A}$

EN = 1: PAD = 3-STATE



BUFFERED OUTPUT, 3-STATE

MACRO NAMING CONVENTION- Q14000

THE EXPANSION OF A MACRO NAME IS GIVEN BELOW:

```
aa[a]nnb
 :   : :
 :   : :
 :   : :
 :   : :
 :   : :
 :   : :
 :   : ---- POWER/FAN-OUT  S - STANDARD      (30 LOADS)
 :   :                        high-fan-out  (50 LOADS)
 :   :                     H - HIGH SPEED    (30 LOADS)
 :   :                     (3-STATE DRIVERS - 8 LOADS)
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FFF - MSI F/F
GT - GENERAL GATES
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MX - MULTIPLEXOR, MUX
REG - MSI REGISTER

IE	ECL input
OE	ECL 10K OUTPUT
UE	ECL 10K Bidirec.
IT	TTL input
OT	TTL output
UT	TTL Bidirectional

FOR TTL I/O MACROS:
00-39 = 100% TTL; OR MIX IN A +5V ONLY CIRCUIT
40-79 = MIX IN A DUAL POWER SUPPLY CIRCUIT

FOR ECL I/O MACROS:
LETTER DESIGNATION FOR ECL 10K AND ECL 100K
ECL MACROS DO NOT VARY WITH I/O MODE

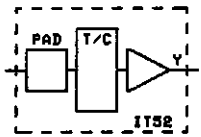
Section 6-2:

TTL Mix Interface

FOR MIXED ECL/TTL MIXED MODE CIRCUITS;
DUAL +5V/-5.2V OR +5V/-4.5V POWER SUPPLIES
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

IT52 1 I/O cell	TTLMIX BUFFERED INPUT			
	S	L	H	
Tpd PAD->Y++	4.50			ns
--	3.09			ns
ICC	1.78			mA I/O
IEE	3.42			mA I/O
FAN-OUT LOAD LIMIT:	50			loads
k-FACTOR RISING	0.025			ns/LU
FALLING	0.030			ns/LU

Y = PAD



AMCC Q14000 MACRO SUMMARY - TTLMIX LIB (803)

FOR MIXED ECL/TTL MIXED MODE CIRCUITS;
DUAL +5V/-5.2V OR +5V/-4.5V POWER SUPPLIES
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

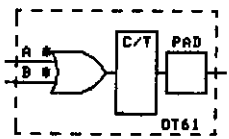
OT61 1 I/O cell TTLMIX OUTPUT WITH OR

		S	L	H	
(1 input changing)					
Tpd	A->PAD ++	2.04			ns
	--	2.30			ns
	B->PAD ++	2.04			ns
	--	2.30			ns
(both inputs changing)					
	->PAD ++	1.91			ns
	--	2.46			ns
ICC		1.45			mA I/O
IEE HIGH		4.25			mA I/O
IEE LOW		2.45			mA I/O

---

* A, B COUNT AS 8 LOADS EACH

PAD = A + B

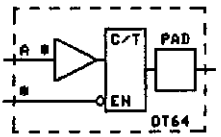


FOR MIXED ECL/TTL MIXED MODE CIRCUITS;
DUAL +5V/-5.2V OR +5V/-4.5V POWER SUPPLIES
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

OT64 1 I/O cell	TTLMIX 3-STATE OUTPUT			
	S	L	H	
Tpd A->PAD++	3.02			ns
--	2.49			ns
(EN->PAD) LZ	1.74			ns
HZ	3.53			ns
ZL	2.68			ns
ZH	3.64			ns
ACTIVE IEE HIGH	4.25			mA I/O
ACTIVE IEE LOW	2.45			mA I/O
ACTIVE ICC	1.45			mA I/O
HIGH-Z IEE	7.05			mA I/O
HIGH-Z ICC	2.90			mA I/O

* A COUNTS AS 8 LOADS
* EN COUNTS AS 16 LOADS

IF EN = 0, PAD = A
IF EN = 1, PAD = HIGH-Z



AMCC Q14000 MACRO SUMMARY - TTLMIX LIB (803)

FOR MIXED ECL/TTL MIXED MODE CIRCUITS;
DUAL +5V/-5.2V OR +5V/-4.5V POWER SUPPLIES
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

UT67 1 I/O cell TTLMIX BIDIRECTIONAL

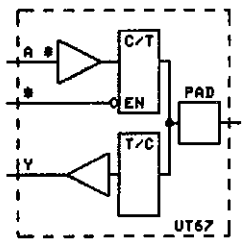
			S	
Tpd	PAD->Y	++	4.37	ns
		--	3.22	ns
	A->PAD	++	2.98	ns
		--	2.46	ns
	EN->PAD	HZ	1.50	ns
		ZH	3.80	ns
		LZ	0.60	ns
		ZL	5.40	ns
ICC			4.70	mA I/O
IEE			10.57	mA I/O
FAN-OUT LOAD LIMIT:		Y	50	loads
k-FACTOR	RISING	Y	0.025	ns/LU
	FALLING		0.030	ns/LU

---

* A COUNTS AS 8 LOADS
* EN COUNTS AS 16 LOADS

EN = 0: PAD = A Y = A

EN = 1: Y = PAD



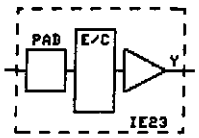
Section 6-3:

ECL Interface

FOR ANY ECL CIRCUITS; SINGLE OR DUAL POWER SUPPLY
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

IE23 1 I/O cell ECL INPUT BUFFER				
		S	H	
Tpd PAD->Y	++	3.43	2.50	ns
	--	2.73	2.04	ns
IEE		2.15	2.80	mA I/O
FAN-OUT LOAD LIMIT:	Y	50	50	loads
k-FACTOR	RISING	0.025	0.025	ns/LU
	FALLING	0.030	0.030	ns/LU

Y = PAD



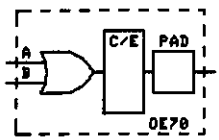
FOR ANY ECL CIRCUITS; SINGLE OR DUAL POWER SUPPLY
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

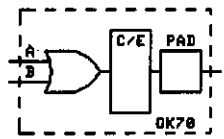
0x70 1 I/O cell	ECL OUTPUT WITH OR		
	OE70 S	OK70 S	
Tpd A,B->PAD ++	0.42	0.44	ns
--	0.79	0.81	ns
IEE	6.30	6.23	mA I/O

* A, B COUNT AS 3 LOADS EACH

PAD = A + B

OE70: ECL 10K
OK70: ECL 100K





FOR ANY ECL CIRCUITS; SINGLE OR DUAL POWER SUPPLY
ALL VALUES ARE TYPICAL AT NOMINAL SUPPLY VOLTAGES
TA = 25oC

UE49 1 I/O cell ECL BIDIRECTIONAL

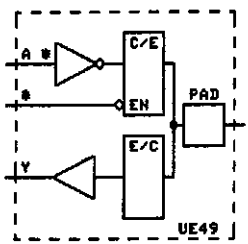
			S	L	H	
Tpd A,EN->PAD	+-		0.53		0.53	ns
	-+		0.38		0.38	ns
PAD->Y	++		3.45		2.55	ns
	--		2.65		2.02	ns
IEE			8.50		9.10	mA I/O
FAN-OUT LOAD LIMIT:		Y	50		50	loads
k-FACTOR RISING		Y	0.025		0.025	ns/LU
FALLING			0.030		0.030	ns/LU

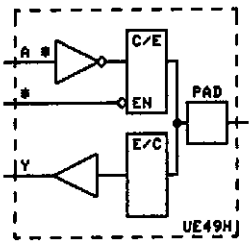
---

* A, EN COUNT AS 3 LOADS EACH

EN = 0: PAD = $\bar{A}$ Y = $\bar{A}$

EN = 1: Y = PAD





Section 6-4:

Basic Logic Macros

ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

EX02 1 B cell EXCLUSIVE OR

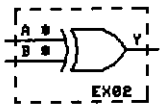
		S	
Tpd	A->Y(B=0)++	1.04	ns
	--	1.67	ns
	B->Y(A=0)++	0.89	ns
	--	1.20	ns
	A->Y(B=1)+-	0.60	ns
	-+	0.69	ns
	B->Y(A=1)+-	1.13	ns
	-+	1.22	ns
FAN-OUT LOAD LIMIT:	Y	30	loads
k-FACTOR	RISING Y	0.025	ns/LU
	FALLING	0.025	ns/LU

---

* A COUNTS AS 3 LOADS
* B COUNTS AS 2 LOADS

Y = A ⊕ B

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0



ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

EX04 1 B cell EXCLUSIVE NOR

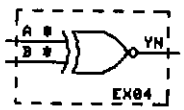
		S	
Tpd A->YN(B=0)	+-	0.62	ns
	-+	0.67	ns
B->YN(A=0)	+-	1.17	ns
	-+	1.34	ns
A->YN(B=1)	++	1.04	ns
	--	1.64	ns
B->YN(A=1)	++	0.76	ns
	--	1.28	ns
FAN-OUT LOAD LIMIT:	YN	30	loads
k-FACTOR RISING	YN	0.025	ns/LU
FALLING		0.025	ns/LU

---

* A COUNTS AS 3 LOADS
* B COUNTS AS 2 LOADS

$$YN = \overline{A \oplus B}$$

A	B	YN
0	0	1
0	1	0
1	0	0
1	1	1



ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

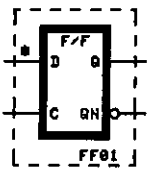
FF01 2 B cells D-FLIP-FLOP

		S	
Tpd C->Q	++	1.68	ns
	+-	1.81	ns
C->QN	++	2.02	ns
	+-	2.33	ns
Tsu (D)		0.60	ns
Th (D)		0.90	ns
PW (C)		1.55	ns
FAN-OUT LOAD LIMIT:		30	loads
k-FACTOR RISING		0.025	ns/LU
FALLING		0.025	ns/LU

---

* D COUNTS AS 2 LOADS

C	D	Qn+1
R	0	0
R	1	1
F	X	Qn
0	X	Qn



ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

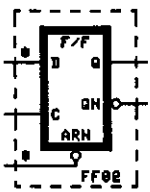
FF02 2 B cells D-FLIP-FLOP WITH ASYNC. RESET

		S	
Tpd C->Q	++	1.77	ns
	+-	1.82	ns
C->QN	++	2.05	ns
	+-	2.50	ns
ARN->Q	--	1.97	ns
ARN->QN	-+	2.16	ns
Tsu (D)		1.10	ns
Th (D)		0.40	ns
Trec(ARN)		0.50	ns
PW (C)		1.70	ns
PW (ARN)		1.95	ns
FAN-OUT LOAD LIMIT:		30	loads
k-FACTOR	RISING	0.025	ns/LU
	FALLING	0.025	ns/LU

---

* ARN, D COUNT AS 2 LOADS EACH

C	D	ARN	Qn+1
R	0	1	0
R	1	1	1
F	X	1	Qn
X	X	0	0



ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

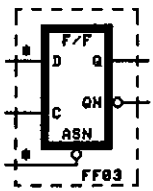
FF03 2 B cells D-FLIP-FLOP WITH ASYNC. SET

		S	
Tpd C->Q	++	1.68	ns
	+-	1.81	ns
C->QN	++	2.20	ns
	+-	2.50	ns
ASN->Q	-+	1.92	ns
ASN->QN	--	1.53	ns
Tsu (D)		0.70	ns
Th (D)		0.80	ns
Trec(ASN)		0.85	ns
PW (C)		1.70	ns
PW (ASN)		1.95	ns
FAN-OUT LOAD LIMIT:		30	loads
k-FACTOR	RISING	0.025	ns/LU
	FALLING	0.025	ns/LU

---

* ASN, D COUNT AS 2 LOADS EACH

C	D	ASN	Qn+1	QNn+1
R	0	1	0	1
R	1	1	1	0
F	X	1	Qn	QNn
X	X	0	1	0



ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

FF04 2 B cells D-FLIP-FLOP WITH ASYNC. SET-RESET

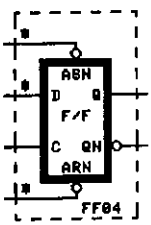
		S	
Tpd C->Q	++	1.60	ns
	+-	1.68	ns
C->QN	++	2.25	ns
	+-	2.31	ns
ASN->Q	-+	0.52	ns
ASN->QN	--	1.29	ns
ARN->Q	--	2.20	ns
ARN->QN	-+	0.54	ns
Tsu (D)		1.00	ns
Th (D)		0.50	ns
Trec(ASN,ARN)		0.00	ns
PW (C)		1.85	ns
PW (ASN,ARN)		1.95	ns
FAN-OUT LOAD LIMIT:		30	loads
k-FACTOR	RISING	0.025	ns/LU
	FALLING	0.025	ns/LU

---

* ASN, ARN, D COUNT AS 2 LOADS EACH

When ARN and ASN go inactive within lns of each other, the outputs of the EWS model for FF14 will go into the "UNKNOWN" state. Tpd delays for recovering from this "UNKNOWN" are the same as those of normal operation as defined above.

C	D	ASN	ARN	Qn+1	QNn+1
R	0	1	1	0	1
R	1	1	1	1	0
F	X	1	1	Qn	QNn
X	X	0	1	1	0
X	X	1	0	0	1
X	X	0	0	X	X



ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

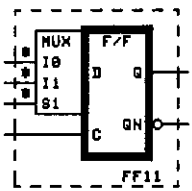
FF11 3 B cells D-FLIP-FLOP WITH 2:1 MUX

		S	
Tpd C->Q	++	2.12	ns
	+-	2.38	ns
C->QN	++	1.75	ns
	+-	1.85	ns
Tsu (I0,I1)		1.50	ns
Tsu (S1)		1.50	ns
Th (I0,I1)		0.00	ns
Th (S1)		0.00	ns
PW (C)		1.55	ns
FAN-OUT LOAD LIMIT:		30	loads
k-FACTOR	RISING	0.025	ns/LU
	FALLING	0.025	ns/LU

---

* I0, I1, S1 COUNT AS 2 LOADS EACH

S1	I0	I1	C	Qn+1	QNn+1
X	X	X	0	Qn	QNn
X	X	X	1	Qn	QNn
0	0	X	R	0	1
0	1	X	R	1	0
1	X	0	R	0	1
1	X	1	R	1	0
X	0	0	R	0	1
X	0	1	R	UNKNOWN	
X	1	0	R	UNKNOWN	
X	1	1	R	1	0
X	X	X	F	Qn	QNn



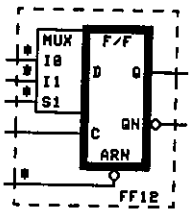
AMCC Q14000 MACRO SUMMARY - FFxx (803A)

ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

FF12 3 B cells D-FLIP-FLOP WITH ASYNC.RESET;2:1 MUX

		S	
Tpd C->Q	++	3.00	ns
	+-	2.40	ns
C->QN	++	1.80	ns
	+-	1.69	ns
ARN->Q	--	1.31	ns
ARN->QN	-+	2.79	ns
Tsu (I0,I1)		1.50	ns
Tsu (S1)		2.70	ns
Th (I0,I1)		0.00	ns
Th (S1)		0.00	ns
Trec(ARN)		0.00	ns
PW (C)		1.70	ns
PW (ARN)		1.95	ns
FAN-OUT LOAD LIMIT:Q,QN		30	loads
k-FACTOR RISING	Q,QN	0.025	ns/LU
FALLING		0.025	ns/LU

* ARN, I0, I1, S1 COUNT AS 2 LOADS EACH



ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

FF12 3 B cells D-FLIP-FLOP WITH ASYNC.RESET;2:1 MUX

ARN	S1	I0	I1	C	Qn+1	QNn+1
1	X	X	X	0	Qn	QNn
1	X	X	X	1	Qn	QNn
1	0	0	X	R	0	1
1	0	1	X	R	1	0
1	1	X	0	R	0	1
1	1	X	1	R	1	0
1	X	0	0	R	0	1
1	X	0	1	R	UNKNOWN	
1	X	1	0	R	UNKNOWN	
1	X	1	1	R	1	0
0	X	X	X	X	0	1
1	X	X	X	F	Qn	QNn

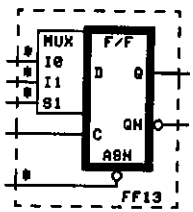
ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

FF13 3 B cells D-FLIP-FLOP WITH ASYNC. SET & 2:1 MUX

		S	
Tpd C->Q	++	2.91	ns
	+-	2.43	ns
C->QN	++	1.92	ns
	+-	1.68	ns
ASN->Q	-+	3.44	ns
ASN->QN	--	2.20	ns
Tsu (I0,I1)		1.60	ns
Tsu (S1)		3.00	ns
Th (I0,I1)		0.00	ns
Th (S1)		0.00	ns
Trec(ASN)		0.00	ns
PW (C)		1.70	ns
PW (ASN)		1.95	ns
FAN-OUT LOAD LIMIT:		30	loads
k-FACTOR	RISING	0.025	ns/LU
	FALLING	0.025	ns/LU

---

* ASN, I0, I1, S1 COUNT AS 2 LOADS EACH



ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

FF13 3 B cells D-FLIP-FLOP WITH ASYNC. SET & 2:1 MUX

ASN	S1	I0	I1	C	Qn+1	QNn+1
1	X	X	X	0	Qn	QNn
1	X	X	X	1	Qn	QNn
1	0	0	X	R	0	1
1	0	1	X	R	1	0
1	1	X	0	R	0	1
1	1	X	1	R	1	0
1	X	0	0	R	0	1
1	X	0	1	R	UNKNOWN	
1	X	1	0	R	UNKNOWN	
1	X	1	1	R	1	0
0	X	X	X	X	1	0
1	X	X	X	F	Qn	QNn

AMCC Q14000 MACRO SUMMARY - FFxx (803A)

ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

FF14 3 B cells D-FF W/2:1MUX ACTIVE LOW ASYNC.SET;RESET

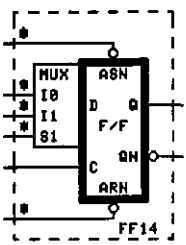
		S	
Tpd C->Q	++	2.36	ns
	+-	2.76	ns
C->QN	++	1.78	ns
	+-	1.88	ns
ARN->Q	--	1.25	ns
ARN->QN	-+	3.05	ns
ASN->Q	-+	2.69	ns
ASN->QN	--	2.34	ns
Tsu (I0,I1)		1.60	ns
Th (I0,I1)		0.00	ns
Tsu (S1)		2.60	ns
Th (S1)		0.00	ns
Trec(ASN,ARN)		0.00	ns
PW (C)		1.85	ns
PW (ASN,ARN)		1.95	ns
FAN-OUT LOAD LIMIT:		30	loads
k-FACTOR	RISING	0.025	ns/LU
	FALLING	0.025	ns/LU

---

* ASN, ARN, I0, I1, S1 COUNT AS 2 LOADS EACH

When ARN and ASN go inactive within 1ns of each other, the outputs of the EWS model for FF14 will go into the "UNKNOWN" state. Some Tpd delays for recovering from this "UNKNOWN" may vary from those of normal operation as defined above.

C	D	ASN	ARN	Qn+1	QNn+1
R	0	1	1	0	1
R	1	1	1	1	0
X	X	0	1	1	0
X	X	1	0	0	1
X	X	0	0	0	1



ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

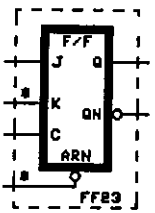
FF23 3 B cells J-K FLIP-FLOP WITH ASYNC. RESET

		S	
Tpd C->Q	++	1.89	ns
	+-	2.04	ns
C->QN	++	2.26	ns
	+-	2.61	ns
ARN->Q	--	2.46	ns
ARN->QN	-+	2.60	ns
Tsu (J,K)		3.10	ns
Th (J,K)		0.00	ns
Trec(ARN)		0.00	ns
PW (C)		1.70	ns
PW (ARN)		1.95	ns
FAN-OUT LOAD LIMIT:		30	loads
k-FACTOR	RISING	0.025	ns/LU
	FALLING	0.025	ns/LU

---

* ARN, K COUNT AS 2 LOADS EACH

C	J	K	ARN	Qn+1	QNn+1
R	0	0	1	Qn	QNn
R	0	1	1	0	1
R	1	0	1	1	0
R	1	1	1	QNn	Qn
F	X	X	1	Qn	QNn
X	X	X	0	0	1



ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

FF24 3 B cells J-K FLIP-FLOP WITH ASYNC. SET-RESET

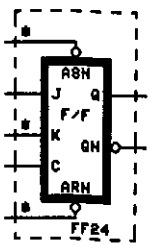
		S	
Tpd C->Q	++	1.72	ns
	+-	1.75	ns
C->QN	++	2.14	ns
	+-	2.62	ns
ARN->Q	--	2.22	ns
ARN->QN	-+	2.52	ns
ASN->Q	-+	2.85	ns
ASN->QN	--	1.15	ns
Tsu (J,K)		3.80	ns
Th (J,K)		0.00	ns
Trec(ASN,ARN)		0.00	ns
PW (C)		1.85	ns
PW (ARN,ASN)		1.95	ns
FAN-OUT LOAD LIMIT:		30	loads
k-FACTOR	RISING	0.025	ns/LU
	FALLING	0.025	ns/LU

---

* ARN, ASN, K COUNT AS 2 LOADS EACH

When ARN and ASN go inactive within 1ns of each other, the outputs of the EWS model for FF24 will go into the "UNKNOWN" state. Some Tpd delays for recovering from this "UNKNOWN" may vary from those of normal operation as defined above.

C	J	K	ASN	ARN	Qn+1	QNn+1
R	0	0	1	1	Qn	QNn
R	0	1	1	1	0	1
R	1	0	1	1	1	0
R	1	1	1	1	QNn	Qn
0	X	X	1	1	Qn	QNn
X	X	X	0	1	1	0
X	X	X	1	0	0	1
X	X	X	0	0	0	0



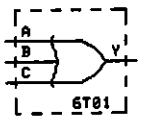
ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

GT01 1 B cell 3-INPUT OR

		S	
(1 input changing)			
Tpd	A->Y++	0.71	ns
	--	2.01	ns
	B->Y++	0.78	ns
	--	2.30	ns
	C->Y++	0.79	ns
	--	2.43	ns
(2 inputs changing)			
	A,B->Y ++	0.53	ns
	--	2.35	ns
	A,C->Y ++	0.53	ns
	--	2.17	ns
	B,C->Y ++	0.58	ns
	--	2.36	ns
(all inputs changing)			
	->Y ++	0.50	ns
	--	2.46	ns
FAN-OUT LOAD LIMIT:	Y	30	loads
k-FACTOR	RISING Y	0.025	ns/LU
	FALLING	0.025	ns/LU

Y = A + B + C

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

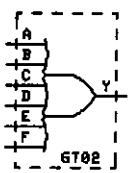


fMAX IS 65MHZ MIL, 82MHZ COM

ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

GT02 1 B cell 6-INPUT OR		
	S	
(1 input changing)		
Tpd A->Y++	0.84	ns
--	2.49	ns
B->Y++	0.80	ns
--	2.26	ns
C->Y++	0.74	ns
--	2.06	ns
D->Y++	0.80	ns
--	2.63	ns
E->Y++	0.71	ns
--	2.41	ns
F->Y++	0.71	ns
--	2.21	ns
(2 inputs changing)		
A,D->Y++	0.61	ns
--	2.84	ns
B,E->Y++	0.61	ns
--	2.60	ns
C,F->Y++	0.57	ns
--	2.40	ns
(all inputs changing)		
->Y++	0.39	ns
--	2.86	ns
FAN-OUT LOAD LIMIT: Y	30	loads
k-FACTOR RISING Y	0.025	ns/LU
FALLING	0.025	ns/LU

Y= A + B + C + D + E + F



fMAX IS 65MHZ MIL, 82MHZ COM

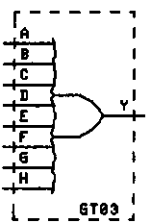
ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

GT03 2 B cells 8-INPUT OR

	S	
(1 input changing)		
Tpd A->Y++	0.84	ns
--	3.26	ns
B->Y++	0.81	ns
--	3.18	ns
C->Y++	0.79	ns
--	2.72	ns
D->Y++	0.74	ns
--	2.38	ns
E->Y++	0.65	ns
--	2.15	ns
F->Y++	0.72	ns
--	2.49	ns
G->Y++	0.74	ns
--	2.95	ns
H->Y++	0.71	ns
--	3.09	ns
(2 inputs changing)		
A,H->Y++	0.58	ns
--	3.52	ns
B,G->Y++	0.59	ns
--	3.42	ns
C,F->Y++	0.58	ns
--	2.94	ns
D,E->Y++	0.55	ns
--	2.61	ns
(all inputs changing)		
->Y++	0.30	ns
--	3.40	ns
FAN-OUT LOAD LIMIT: Y	30	loads
k-FACTOR RISING Y	0.025	ns/LU
FALLING	0.025	ns/LU

Y= A + B + C + D + E + F + G + H

fMAX IS 65MHZ MIL, 82MHZ COM

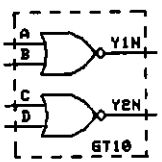


ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

GT10 1 B cell DUAL 2-INPUT NOR		
	S	
(1 input changing)		
Tpd A->Y1N+-	0.51	ns
-+	0.92	ns
B->Y1N+-	0.48	ns
-+	0.82	ns
C->Y2N+-	0.47	ns
-+	0.83	ns
D->Y2N+-	0.49	ns
-+	0.93	ns
(2 inputs changing)		
A,B->Y1N+-	0.34	ns
-+	1.00	ns
C,D->Y2N+-	0.33	ns
-+	1.00	ns
FAN-OUT LOAD LIMIT:	30	loads
k-FACTOR RISING	0.030	ns/LU
FALLING	0.025	ns/LU

$$Y1N = \overline{\overline{A} + B}$$

$$Y2N = \overline{\overline{C} + D}$$

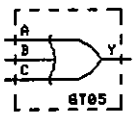


ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

GT05 1 B cell 3-INPUT OR

		S	
Tpd	A->Y++	1.02	ns
	--	1.47	ns
	B->Y++	0.94	ns
	--	1.46	ns
	C->Y++	1.11	ns
	--	1.01	ns
(2 INPUTS CHANGING)			
	A,B->Y++	0.75	ns
	--	1.67	ns
	B,C->Y++	0.73	ns
	--	1.47	ns
	A,C->Y++	0.77	ns
	--	1.49	ns
(ALL INPUTS CHANGING)			
	A,B,C->Y ++	0.61	ns
	--	1.69	ns
FAN-OUT LOAD LIMIT:	Y	30	loads
k-FACTOR	RISING Y	0.025	ns/LU
	FALLING	0.025	ns/LU

Y= A + B + C



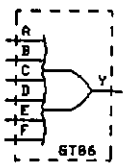
A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

GT06 2 B cells 6-INPUT OR

		S	
Tpd	A->Y++	1.31	ns
	--	1.51	ns
	B->Y++	1.23	ns
	--	1.52	ns
	C->Y++	1.40	ns
	--	1.61	ns
	D->Y++	1.33	ns
	--	1.60	ns
	E->Y++	1.63	ns
	--	1.62	ns
	F->Y++	1.54	ns
	--	1.61	ns
(ALL INPUTS CHANGING)			
	A,B,C,D,E,F->Y++	0.57	ns
	--	2.05	ns
FAN-OUT LOAD LIMIT:	Y	30	loads
k-FACTOR	RISING Y	0.025	ns/LU
	FALLING	0.025	ns/LU

Y = A + B + C + D + E + F



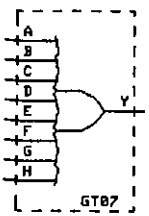
ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

GT07 3 B cells 8-INPUT OR

		S	
Tpd	A->Y++	2.12	ns
	--	2.17	ns
	B->Y++	2.05	ns
	--	2.16	ns
	C->Y++	2.46	ns
	--	2.21	ns
	D->Y++	2.38	ns
	--	2.20	ns
	E->Y++	2.33	ns
	--	2.31	ns
	F->Y++	2.53	ns
	--	2.29	ns
	G->Y++	2.29	ns
	--	2.28	ns
	H->Y++	2.23	ns
	--	2.26	ns
FAN-OUT LOAD LIMIT:	Y	30	loads
k-FACTOR	RISING Y	0.025	ns/LU
	FALLING	0.025	ns/LU

Y = A + B + C + D + E + F + G + H

A	B	C	D	E	F	G	H	Y
0	0	0	0	0	0	0	0	0
ALL OTHER COMBINATIONS								1

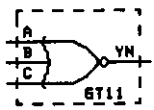


ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

GT11 1 B cell 3-INPUT NOR

		S	
(1 input changing)			
Tpd A->YN	+-	0.54	ns
	-+	1.77	ns
B->YN	+-	0.55	ns
	-+	1.53	ns
C->YN	+-	0.50	ns
	-+	1.18	ns
(2 inputs changing)			
A,B->YN	+-	0.37	ns
	-+	1.70	ns
A,C->YN	+-	0.35	ns
	-+	1.25	ns
B,C->YN	+-	0.37	ns
	-+	1.51	ns
(all inputs changing)			
->YN	+-	0.30	ns
	-+	1.64	ns
FAN-OUT LOAD LIMIT: YN		30	loads
k-FACTOR RISING	YN	0.035	ns/LU
FALLING		0.025	ns/LU

$$YN = \overline{A + B + C}$$



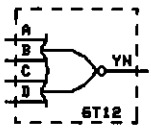
fMAX IS 65MHZ MIL, 82MHZ COM

ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

GT12 1 B cell 4-INPUT NOR

		S	
(1 input changing)			
Tpd	A->YN+-	0.58	ns
	-+	2.72	ns
	B->YN+-	0.57	ns
	-+	2.67	ns
	C->YN+-	0.57	ns
	-+	2.12	ns
	D->YN+-	0.54	ns
	-+	1.45	ns
(2 inputs changing)			
	A,B->YN+-	0.35	ns
	-+	2.91	ns
	A,C->YN+-	0.36	ns
	-+	2.24	ns
	A,D->YN+-	0.36	ns
	-+	1.49	ns
	B,C->YN+-	0.39	ns
	-+	2.45	ns
	B,D->YN+-	0.39	ns
	-+	1.60	ns
	C,D->YN+-	0.39	ns
	-+	2.02	ns
(all inputs changing)			
	->YN+-	0.28	ns
	-+	2.47	ns
FAN-OUT LOAD LIMIT:	YN	30	loads
k-FACTOR	RISING YN	0.040	ns/LU
	FALLING	0.030	ns/LU

$$YN = \overline{A + B + C + D}$$

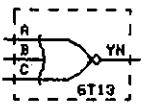


fMAX IS 65MHZ MIL, 82MHZ COM

ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

GT13	1 B Cell	3-INPUT NOR	
		S	
(1 INPUT CHANGING)			
Tpd	A->YN+-	1.20	ns
	-+	1.96	ns
	B->YN+-	1.13	ns
	-+	1.92	ns
	C->YN+-	1.25	ns
	-+	1.52	ns
(2 INPUTS CHANGING)			
	A,B->YN+-	0.97	ns
	-+	2.12	ns
	A,C->YN+-	0.91	ns
	-+	2.00	ns
	B,C->YN+-	0.87	ns
	-+	1.97	ns
(ALL INPUTS CHANGING)			
	A,B,C->YN+-	0.76	ns
	-+	2.16	ns
FAN-OUT LOAD LIMIT: YN		30	loads
k-FACTOR	RISING YN	0.025	ns/LU
	FALLING	0.025	ns/LU

$$YN = \overline{A + B + C}$$

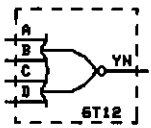


ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

GT12 1 B cell 4-INPUT NOR

		S	
(1 input changing)			
Tpd	A->YN+-	0.58	ns
	-+	2.72	ns
	B->YN+-	0.57	ns
	-+	2.67	ns
	C->YN+-	0.57	ns
	-+	2.12	ns
	D->YN+-	0.54	ns
	-+	1.45	ns
(2 inputs changing)			
	A,B->YN+-	0.35	ns
	-+	2.91	ns
	A,C->YN+-	0.36	ns
	-+	2.24	ns
	A,D->YN+-	0.36	ns
	-+	1.49	ns
	B,C->YN+-	0.39	ns
	-+	2.45	ns
	B,D->YN+-	0.39	ns
	-+	1.60	ns
	C,D->YN+-	0.39	ns
	-+	2.02	ns
(all inputs changing)			
	->YN+-	0.28	ns
	-+	2.47	ns
FAN-OUT LOAD LIMIT:	YN	30	loads
k-FACTOR	RISING YN	0.040	ns/LU
	FALLING	0.030	ns/LU

$$YN = \overline{A + B + C + D}$$



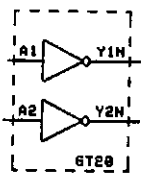
fMAX IS 65MHZ MIL, 82MHZ COM

ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

GT20 1 B cell DUAL INVERTER			
		S	
Tpd A1->Y1N	+-	0.36	ns
	-+	0.47	ns
A2->Y2N	+-	0.36	ns
	-+	0.47	ns
FAN-OUT LOAD LIMIT:		30	loads
k-FACTOR	RISING	0.025	ns/LU
	FALLING	0.025	ns/LU

$Y1N = \overline{A1}$

$Y2N = \overline{A2}$

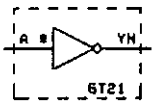


ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

GT21 1 B cell HIGH-FAN-OUT INVERTING DRIVER

			S	
Tpd A->YN	+-		0.40	ns
	-+		0.66	ns
FAN-OUT LOAD LIMIT:		YN	50	loads
k-FACTOR	RISING	YN	0.025	ns/LU
	FALLING		0.025	ns/LU

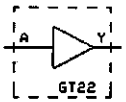
YN = $\bar{A}$



ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

GT22 1 B cell HIGH-FAN-OUT DRIVER			
		S	
Tpd A->Y++		0.86	ns
--		1.16	ns
FAN-OUT LOAD LIMIT:	Y	50	loads
k-FACTOR RISING	Y	0.025	ns/LU
FALLING		0.025	ns/LU

Y = A



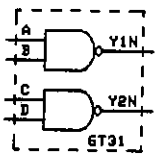
ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

GT31 1 B cell DUAL 2-INPUT NAND

		S	
(1 input changing)			
Tpd A->Y1N,C->Y2N	+-	0.47	ns
	-+	0.52	ns
B->Y1N,D->Y2N	+-	0.59	ns
	-+	0.48	ns
(both inputs changing)			
A,B->Y1N,C,D->Y2N	+-	0.68	ns
	-+	0.30	ns
FAN-OUT LOAD LIMIT:		30	loads
k-FACTOR RISING		0.025	ns/LU
FALLING		0.025	ns/LU

$Y1N = \overline{A \cdot B}$

$Y2N = \overline{C \cdot D}$

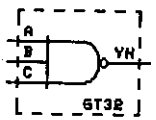


ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

GT32 1 B cell 3-INPUT NAND

		S	
(1 input changing)			
Tpd	A->YN+-	0.93	ns
	-+	0.60	ns
	B->YN+-	0.79	ns
	-+	0.60	ns
	C->YN+-	0.63	ns
	-+	0.62	ns
(2 inputs changing)			
	A,B->YN+-	1.06	ns
	-+	0.33	ns
	A,C->YN+-	1.03	ns
	-+	0.34	ns
	B,C->YN+-	0.86	ns
	-+	0.37	ns
(all inputs changing)			
	->YN+-	1.15	ns
	-+	0.26	ns
FAN-OUT LOAD LIMIT:	YN	30	loads
k-FACTOR	RISING YN	0.025	ns/LU
	FALLING	0.025	ns/LU

$YN = \overline{A \cdot B \cdot C}$

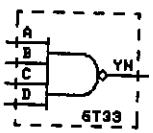


ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

GT33 1 B cell 4-INPUT NAND

		S	
(1 input changing)			
Tpd	A->YN+-	1.20	ns
	-+	0.60	ns
	B->YN+-	1.08	ns
	-+	0.60	ns
	C->YN+-	0.89	ns
	-+	0.63	ns
	D->YN+-	0.66	ns
	-+	0.63	ns
(2 inputs changing)			
	A,B->YN+-	1.44	ns
	-+	0.22	ns
	A,C->YN+-	1.29	ns
	-+	0.34	ns
	A,D->YN+-	1.27	ns
	-+	0.33	ns
	B,C->YN+-	1.20	ns
	-+	0.37	ns
	B,D->YN+-	1.15	ns
	-+	0.37	ns
	C,D->YN+-	0.93	ns
	-+	0.37	ns
(all inputs changing)			
	->YN+-	1.44	ns
	-+	0.22	ns
FAN-OUT LOAD LIMIT:	YN	30	loads
k-FACTOR	RISING YN	0.025	ns/LU
	FALLING	0.030	ns/LU

$YN = \overline{A \cdot B \cdot C \cdot D}$



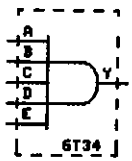
fMAX IS 65MHZ MIL, 82MHZ COM

ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

GT34 1 B cell 5-INPUT AND

		S	
(1 input changing)			
Tpd	A->Y++	0.98	ns
	--	1.23	ns
	B->Y++	1.28	ns
	--	1.18	ns
	C->Y++	1.37	ns
	--	1.08	ns
	D->Y++	1.44	ns
	--	1.27	ns
	E->Y++	1.56	ns
	--	1.54	ns
(2 inputs changing)			
	A,B->Y++	1.36	ns
	--	0.69	ns
	A,C->Y++	1.43	ns
	--	0.90	ns
	A,D->Y++	1.51	ns
	--	0.97	ns
	A,E->Y++	1.62	ns
	--	1.00	ns
	B,C->Y++	1.62	ns
	--	1.00	ns
	B,D->Y++	1.51	ns
	--	1.08	ns
	B,E->Y++	1.62	ns
	--	1.16	ns
	C,D->Y++	1.50	ns
	--	0.77	ns
	C,E->Y++	1.48	ns
	--	0.76	ns
	D,E->Y++	1.55	ns
	--	0.85	ns
(all inputs changing)			
	->Y++	1.66	ns
	--	0.57	ns
FAN-OUT LOAD LIMIT: Y		30	loads
k-FACTOR	RISING Y	0.030	ns/LU
	FALLING	0.025	ns/LU

Y = A*B*C*D*E



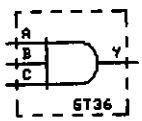
ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

GT36 1 B cell 3-INPUT AND

		S	
(1 input changing)			
Tpd	A->Y++	1.02	ns
	--	1.04	ns
	B->Y++	1.17	ns
	--	1.36	ns
	C->Y++	1.22	ns
	--	1.53	ns
(2 inputs changing)			
	A,B->Y++	1.17	ns
	--	0.74	ns
	A,C->Y++	1.12	ns
	--	0.73	ns
	B,C->Y++	1.32	ns
	--	0.88	ns
(all inputs changing)			
	->Y++	1.23	ns
	--	0.61	ns
FAN-OUT LOAD LIMIT: Y		30	loads
k-FACTOR	RISING Y	0.025	ns/LU
	FALLING	0.025	ns/LU

Y = A·B·C

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

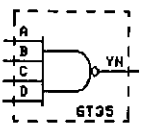


ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

GT35 1 B cell 4-INPUT AND

		S	
(1 INPUT CHANGING)			
Tpd	A->YN-+	0.70	ns
	+-	0.47	ns
	B->YN-+	0.79	ns
	+-	0.61	ns
	C->YN-+	0.89	ns
	+-	0.79	ns
	D->YN-+	0.95	ns
	+-	0.87	ns
(2 INPUTS CHANGING)			
	A,B->YN-+	0.46	ns
	+-	0.68	ns
	A,C->YN-+	0.43	ns
	+-	0.73	ns
	A,D->YN-+	0.41	ns
	+-	0.75	ns
	B,C->YN-+	0.48	ns
	+-	0.78	ns
	B,D->YN-+	0.45	ns
	+-	0.80	ns
	C,D->YN-+	0.50	ns
	+-	0.96	ns
(ANY 3 INPUTS CHANGING)			
	+-	0.91	ns
	-+	0.37	ns
(ALL INPUTS CHANGING)			
	+-	0.99	ns
	-+	0.28	ns
FAN-OUT LOAD LIMIT: YN		30	loads
k-FACTOR	RISING YN	0.025	ns/LU
	FALLING	0.030	ns/LU

$YN = \overline{ABCD}$

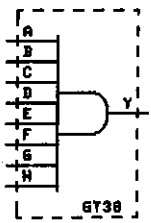


ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

GT38 2 B cells 8-INPUT AND

		S	
(1 input changing)			
Tpd	A->Y++	1.43	ns
	--	1.12	ns
	B->Y++	1.56	ns
	--	1.29	ns
	C->Y++	1.79	ns
	--	1.61	ns
	D->Y++	1.88	ns
	--	1.71	ns
	E->Y++	1.58	ns
	--	1.23	ns
	F->Y++	1.75	ns
	--	1.38	ns
	G->Y++	1.97	ns
	--	1.66	ns
	H->Y++	2.06	ns
	--	1.78	ns
(2 inputs changing)			
	A,E->Y++	1.72	ns
	--	0.99	ns
	B,F->Y++	1.95	ns
	--	1.18	ns
	C,G->Y++	2.13	ns
	--	1.47	ns
	D,H->Y++	2.17	ns
	--	1.56	ns
(all inputs changing)			
	->Y++	2.22	ns
	--	0.49	ns
FAN-OUT LOAD LIMIT:	Y	30	loads
k-FACTOR	RISING Y	0.030	ns/LU
	FALLING	0.025	ns/LU

$Y = A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H$



ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

GT41 1 B cell 2-WIDE 1-2 INPUT AND-OR INVERT

			S	
Tpd	A->YN-+		0.90	ns
		+-	0.82	ns
	B->YN-+		0.93	ns
		+-	0.67	ns
	C->YN-+		1.05	ns
		+-	0.75	ns
FAN-OUT LOAD LIMIT:		YN	30	loads
k-FACTOR	RISING	YN	0.030	ns/LU
	FALLING		0.025	ns/LU

$$YN = \overline{(A \cdot B) + C}$$

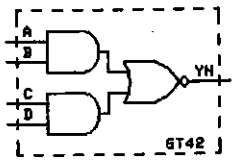
ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

GT42 1 B cell 2-WIDE 2-2 INPUT AND-OR INVERT

		S	
Tpd	A->YN+-	0.90	ns
	-+	0.89	ns
	B->YN+-	0.77	ns
	-+	0.91	ns
	C->YN+-	1.14	ns
	-+	1.19	ns
	D->YN+-	1.00	ns
	-+	1.20	ns
FAN-OUT LOAD LIMIT:	YN	30	loads
k-FACTOR	RISING	YN 0.030	ns/LU
	FALLING	0.030	ns/LU

$$YN = \overline{A \cdot B + C \cdot D}$$

A	B	C	D	YN
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

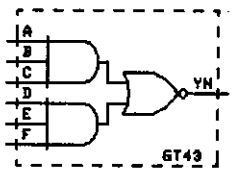


ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

GT43 1 B cell 2-WIDE 3-3 INPUT AND-OR INVERT

			S	
Tpd	A->YN+-		1.16	ns
		-+	0.82	ns
	B->YN+-		1.01	ns
		-+	0.84	ns
	C->YN+-		0.83	ns
		-+	0.86	ns
	D->YN+-		1.85	ns
		-+	1.45	ns
	E->YN+-		1.72	ns
		-+	1.45	ns
	F->YN+-		1.53	ns
		-+	1.47	ns
FAN-OUT LOAD LIMIT:		YN	30	loads
k-FACTOR	RISING	YN	0.035	ns/LU
	FALLING		0.040	ns/LU

$$YN = \overline{(A \cdot B \cdot C)} + \overline{(D \cdot E \cdot F)}$$

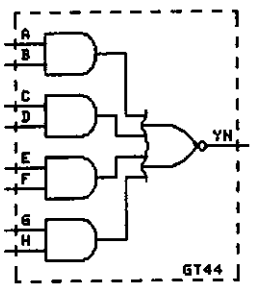


ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

GT44 2 B cells 4-WIDE 2-2-2-2 INPUT AND-OR INVERT

		S	
Tpd	A->YN+-	1.52	ns
	-+	3.12	ns
	B->YN+-	1.32	ns
	-+	3.19	ns
	C->YN+-	1.12	ns
	-+	3.06	ns
	D->YN+-	1.25	ns
	-+	3.09	ns
	E->YN+-	1.20	ns
	-+	1.94	ns
	F->YN+-	1.02	ns
	-+	1.97	ns
	G->YN+-	0.88	NS
	-+	1.10	ns
	H->YN+-	0.77	ns
	-+	1.12	ns
FAN-OUT LOAD LIMIT:	YN	30	loads
k-FACTOR	RISING YN	0.045	ns/LU
	FALLING	0.035	ns/LU

$$YN = \overline{(A \cdot B)} + \overline{(C \cdot D)} + \overline{(E \cdot F)} + \overline{(G \cdot H)}$$



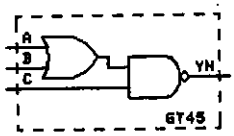
fMAX IS 65MHZ MIL, 82MHZ COM

ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

GT45 1 B cell 2-WIDE 1-2 INPUT OR-AND INVERT

		S	
Tpd	A->YN+-	0.67	ns
	-+	0.94	ns
	B->YN+-	0.82	ns
	-+	1.15	ns
	C->YN+-	0.72	ns
	-+	0.55	ns
FAN-OUT LOAD LIMIT:	YN	30	loads
k-FACTOR	RISING YN	0.030	ns/LU
	FALLING	0.030	ns/LU

$$YN = \overline{(A+B)} \cdot C$$



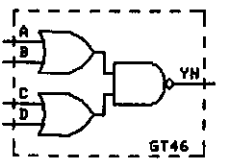
ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

GT46 1 B cell 2-WIDE 2-2 INPUT OR-AND INVERT

			S	
Tpd	A->YN+-		0.86	ns
		-+	1.13	ns
	B->YN+-		0.92	ns
		-+	1.22	ns
	C->YN+-		0.71	ns
		-+	1.19	ns
	D->YN+-		0.77	ns
		-+	1.27	ns
FAN-OUT LOAD LIMIT:		YN	30	loads
k-FACTOR	RISING	YN	0.030	ns/LU
	FALLING		0.030	ns/LU

$$YN = \overline{(A+B)\cdot(C+D)}$$

A	B	C	D	YN
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

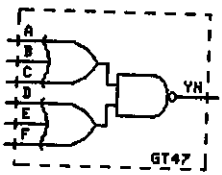


ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

GT47 2 B cells 2-WIDE 3-3 INPUT OR-AND INVERT

			S	
Tpd	A->YN+-		0.92	ns
		-+	1.63	ns
	B->YN+-		0.97	ns
		-+	1.93	ns
	C->YN+-		0.98	ns
		-+	2.13	ns
	D->YN+-		0.76	ns
		-+	1.71	ns
	E->YN+-		0.81	ns
		-+	2.01	ns
	F->YN+-		0.81	ns
		-+	2.21	ns
FAN-OUT LOAD LIMIT:		YN	30	loads
k-FACTOR	RISING	YN	0.040	ns/LU
	FALLING		0.030	ns/LU

$$YN = \overline{(A+B+C)} \cdot \overline{(D+E+F)}$$



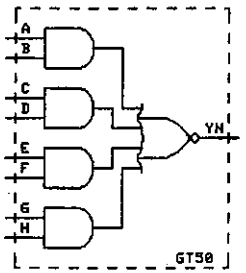
fMAX IS 65MHZ MIL, 62MHZ COM

ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

GT50 2 B cells 4 WIDE 2-2-2-2 INPUT AND - OR INVERT

		S	
Tpd	A->YN+-	1.77	ns
	-+	2.15	ns
	B->YN+-	1.88	ns
	-+	2.70	ns
	C->YN+-	1.98	ns
	-+	2.22	ns
	D->YN+-	2.06	ns
	-+	2.73	ns
	E->YN+-	2.04	ns
	-+	2.14	ns
	F->YN+-	2.16	ns
	-+	2.67	ns
	G->YN+-	2.26	ns
	-+	2.22	ns
	H->YN+-	2.36	ns
	-+	2.71	ns
FAN-OUT LOAD LIMIT:	YN	30	loads
k-FACTOR	RISING YN	0.025	ns/LU
	FALLING	0.025	ns/LU

$$YN = \overline{AB + CD + EF + GH}$$

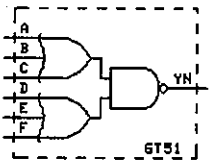


ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

GT51 2 B cells 2-WIDE 3-3 INPUT OR - AND INVERT

			S	
Tpd	A->YN+-		1.15	ns
		-+	1.99	ns
	B->YN+-		1.29	ns
		-+	2.06	ns
	C->YN+-		1.47	ns
		-+	2.16	ns
	D->YN+-		1.19	ns
		-+	2.16	ns
	E->YN+-		1.33	ns
		-+	2.23	ns
	F->YN+-		1.51	ns
		-+	2.33	ns
FAN-OUT LOAD LIMIT:		YN	30	loads
k-FACTOR	RISING	YN	0.030	ns/LU
	FALLING		0.025	ns/LU

$$YN = \overline{(A+B+C)(D+E+F)}$$

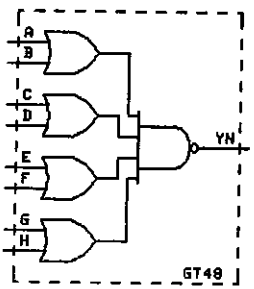


ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

GT48 2 B cells 4-WIDE 2-2-2-2 INPUT OR-AND INVERT

		S	
Tpd	A->YN+-	1.57	ns
	-+	1.51	ns
	B->YN+-	1.62	ns
	-+	1.55	ns
	C->YN+-	1.38	ns
	-+	1.55	ns
	D->YN+-	1.46	ns
	-+	1.60	ns
	E->YN+-	1.17	ns
	-+	1.60	ns
	F->YN+-	1.25	ns
	-+	1.64	ns
	G->YN+-	0.94	ns
	-+	1.63	ns
	H->YN+-	0.99	ns
	-+	1.67	ns
FAN-OUT LOAD LIMIT: YN		30	loads
k-FACTOR	RISING YN	0.035	ns/LU
	FALLING	0.040	ns/LU

$$YN = \overline{(A+B)\cdot(C+D)\cdot(E+F)\cdot(G+H)}$$



ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

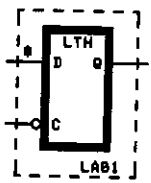
LA01 1 B cell LATCH TRANSPARENT LOW

		S	
Tpd D->Q	++	0.96	ns
	--	1.32	ns
C->Q	-+	2.02	ns
	--	2.33	ns
Tsu (D)		1.00	ns
Th (D)		0.50	ns
PW (C)		1.55	ns
FAN-OUT LOAD LIMIT:		30	loads
k-FACTOR	RISING	0.025	ns/LU
	FALLING	0.025	ns/LU

---

* D COUNTS AS 2 LOADS

C	D	Qn+1
0	0	0
0	1	1
1	X	Qn



ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

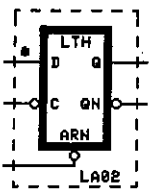
LA02 1 B cell LATCH WITH ACTIVE LOW RESET

		S	
Tpd D->Q	++	1.43	ns
	--	1.17	ns
D->QN	-+	0.66	ns
	+-	0.86	ns
C->Q	-+	2.47	ns
	--	2.20	ns
C->QN	-+	1.69	ns
	--	1.90	ns
ARN->Q	--	1.03	ns
ARN->QN	-+	0.55	ns
Tsu (D)		1.00	ns
Th (D)		0.50	ns
Trec(ARN)		0.00	ns
PW (C)		1.70	ns
PW (ARN)		1.95	ns
FAN-OUT LOAD LIMIT:		30	loads
k-FACTOR	RISING	0.025	ns/LU
	FALLING	0.025	ns/LU

---

* D COUNTS AS 2 LOADS

C	D	ARN	Qn+1	QNn+1
0	0	1	0	1
0	1	1	1	0
1	X	1	Qn	QNn
X	X	0	0	1



ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

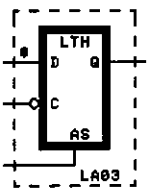
LA03 1 B cell LATCH WITH SET

		S	
Tpd C->Q	-+	1.93	ns
	--	2.54	ns
D->Q	++	0.87	ns
	--	1.51	ns
AS->Q	++	0.73	ns
	--	1.41	ns
Tsu (D)		0.50	ns
Th (D)		1.00	ns
Trec(AS)		2.50	ns
PW (C)		1.70	ns
PW (AS)		1.95	ns
FAN-OUT LOAD LIMIT:		30	loads
k-FACTOR	RISING	0.025	ns/LU
	FALLING	0.025	ns/LU

---

* D COUNTS AS 2 LOADS

C	D	AS	Qn+1
0	0	0	0
0	1	0	1
1	X	0	Qn
X	X	1	1



Section 6-5:

MSI Macros

ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

ADD283 14 B cells 4-BIT CARRY LOOK-AHEAD ADDER; CO

		S	
Tpd CI->SI	++	3.82	ns
	+-	3.95	ns
	-+	4.33	ns
	--	4.61	ns
CI->CO	++	2.25	ns
	--	2.71	ns
Ai,Bi->CO	++	3.41	ns
	--	3.73	ns
A3,B3->CO	++	2.88	ns
	--	2.82	ns
A0,B0->S0	++	2.67	ns
	+-	3.25	ns
	-+	3.11	ns
	--	3.35	ns
A0,B0->S1	++	2.95	ns
	+-	3.03	ns
	-+	3.44	ns
	--	3.68	ns
A0,B0->S2	++	3.72	ns
	+-	3.90	ns
	-+	4.42	ns
	--	4.32	ns
A0,B0->S3	++	4.26	ns
	+-	4.41	ns
	-+	4.54	ns
	--	5.00	ns
A1,B1->S1	++	2.84	ns
	+-	3.26	ns
	-+	3.11	ns
	--	3.54	ns
A1,B1->S2	++	3.65	ns
	+-	3.74	ns
	-+	3.72	ns
	--	3.95	ns
A1,B1->S3	++	4.40	ns
	+-	4.48	ns
	-+	4.40	ns
	--	4.69	ns
A2,B2->S2	++	2.89	ns
	+-	3.24	ns
	-+	3.12	ns
	--	3.60	ns

i= 0,1,2

continued on the next page

ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

ADD283 14 B cells 4-BIT CARRY LOOK-AHEAD ADDER; CO

		S	
A2,B2->S3	++	4.07	ns
	+-	4.19	ns
	-+	3.28	ns
	--	3.54	ns
A3,B3->S3	++	2.85	ns
	+-	3.07	ns
	-+	3.01	ns
	--	3.21	ns

i= 0,1,2

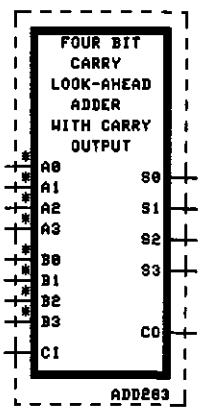
FAN-OUT LOAD LIMIT:	30	loads
k-FACTOR RISING	0.025	ns/LU
FALLING	0.025	ns/LU

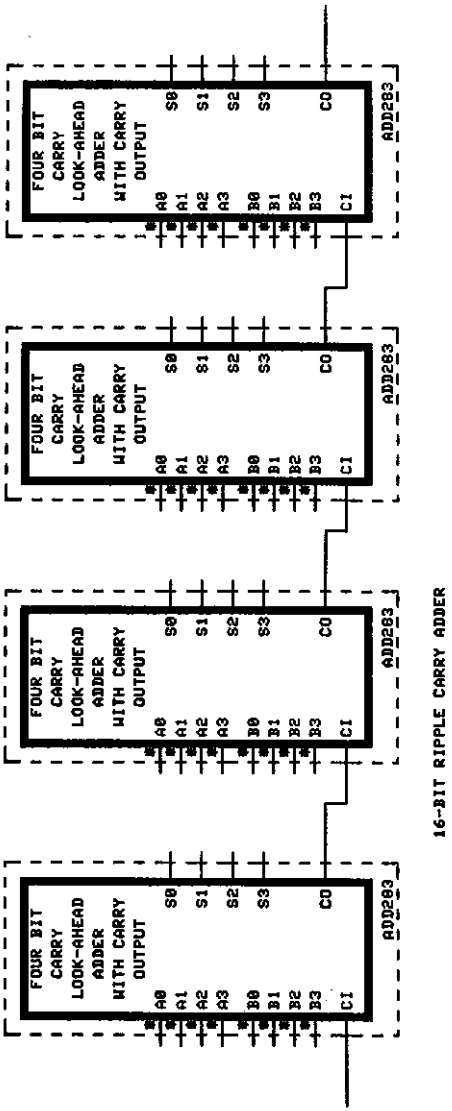
---

* A3,A2,A1,A0,B3,B2,B1,B0 COUNT AS 2 LOADS EACH

ADD283 is a fast 4-bit binary full adder with carry look-ahead. Add283 adds 2 4-bit binary words (A3-A0, B3-B0) plus the incoming carry (CI) and generates the binary sum bits (S3-S0) and the carry-out (CO). ADD283 operates with either active-high or active-low operands (positive or negative logic).

				CI
	A3	A2	A1	A0
+	B3	B2	B1	B0
CO	S3	S2	S1	S0




FOUR BIT
CARRY
LOOK-AHEAD
ADDER
WITH CARRY
OUTPUT
A0
A1
A2
A3
B0
B1
B2
B3
CI
S0
S1
S2
S3
CO
ADD283
16-BIT RIPPLE CARRY ADDER

ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

CMP688 6 B cells 8-BIT MAGNITUDE COMPARATOR

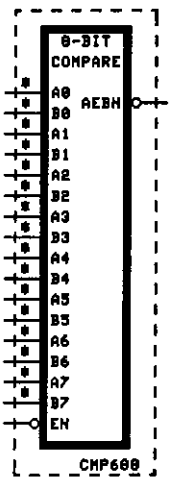
		S	
Tpd	Ai->AEBN++	1.40	ns
	-+	1.03	ns
	+-	3.94	ns
	--	5.08	ns
	Bi->AEBN++	1.21	ns
	-+	1.54	ns
	+-	4.53	ns
	--	4.47	ns
	EN->AEBN++	0.76	ns
	--	2.34	ns

i = 0,1,2,3,4,5,6,7

FAN-OUT LOAD LIMIT:		30	loads
k-FACTOR	RISING	0.025	ns/LU
	FALLING	0.025	ns/LU

---

* ALL Ai, Bi INPUTS COUNT AS 2 LOADS EACH



ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

CMP688 6 B cells 8-BIT MAGNITUDE COMPARATOR

CMP688 compares A7-A0 and B7-B0, the magnitudes of 2 8-bit binary words. The output (AEBN) is LOW if the magnitudes of the input words are equal. For all other conditions, the output is HIGH. When the enable input (EN) is HIGH, it overrides the result of the comparison and forces the output HIGH.

FUNCTION TABLE

INPUTS DATA Ai;Bi	ENABLE EN	OUTPUT AEBN	where A and B are binary words
A=B	0	0	if all Ai bits equal all Bi bits
A>B	0	1	if the sum of the Ai bits Greater than the sum of the Bi bits
A<B	0	1	if the sum of the Ai bits Less than the sum of the Bi bits
X	1	1	if CMP688 is disabled

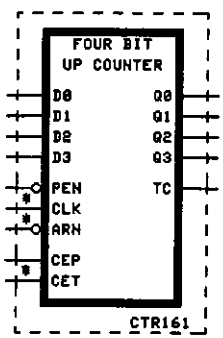
ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

CTR161 16 B cells 4-BIT UP-CNTR; AR; LOAD & ENABLE

		S TYP	MIL	COM	
Tpd CLK->Qi	++	1.94			ns
	+-	1.93			ns
CLK->TC	++	4.41			ns
	+-	2.55			ns
ARN->Qi	--	2.76			ns
ARN->TC	--	3.37			ns
CET->TC	++	1.49			ns
	--	1.55			ns
i = 0,1,2,3					
Tsu (Di)		2.90			ns
Th (Di)		0.00			ns
i=0,1,2,3					
Tsu (PEN)		4.90			ns
Th (PEN)		0.00			ns
Tsu (CEP)		6.10			ns
Th (CEP)		0.00			ns
Trec(ARN)		1.45			ns
PW (ARN)		2.46			ns
PW (CLK)		1.95	3.80	3.02	ns
FAN-OUT LOAD LIMIT:		30			loads
k-FACTOR	RISING Qi	0.025			ns/LU
	FALLING	0.025			ns/LU
	RISING TC	0.030			ns/LU
	FALLING	0.025			ns/LU
MAXIMUM FREQUENCY OF OPERATION (fMAX)			56	70	MHz

---

* CLK, ARN, CET COUNT AS 2 LOADS EACH



ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

CTR161 16 B cells 4-BIT UP-CNTR; AR; LOAD & ENABLE

CTR161 is synchronously presettable for applications such as programmable dividers. The LOW-active preset enable input (PEN) allows parallel loading of this counter with the contents of the data inputs (D3-D0) on the next rising edge of the clock input (CLK). This macro provides two types of count enable inputs (CEP, CET), and generates the terminal count indicator (TC) to allow versatility in multi-stage synchronous counting. TC signals the following stage to advance on the next clock. Either CEP or CET will stop the counter from counting when disabled. CET will also force TC to zero. CTR161 has an asynchronous master reset (ARN) that overrides all other inputs and forces the outputs (Q3-Q0, TC) LOW.

FUNCTION TABLE

INPUTS						OUTPUTS
RESET ARN	LOAD PEN	ENABLE CEP	ENABLE CET	CLOCK CLK	Qi	TC
0	X	X	X	X	RESET Qi=0	0
1	0	X	1	R	LOAD	If sum Qi=15, TC=1 else TC=0
1	0	X	0	R	LOAD	0
1	1	0	1	X	STOP	If sum Qi=15, TC=1 else TC=0
1	1	X	0	X	STOP	0
1	1	1	1	R	COUNT UP	If sum Qi=15, TC=1 else TC=0
1	1	1	1	F	NO CHANGE	If sum Qi=15, TC=1 else TC=0

TC = Q3.Q2.Q1.Q0.CET . = AND
X = DON'T CARE
R = RISING EDGE
F = FALLING EDGE

AMCC Q14000 MACRO SUMMARY - CTRxx (803A)

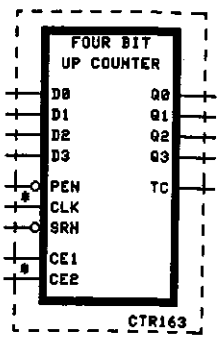
ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

CTR163 14 B cells 4-BIT CNTR; SR

		S TYP	MIL	COM	
Tpd CLK->Qi	++	1.82			ns
	+-	1.90			ns
CLK->TC	++	4.51			ns
	+-	2.65			ns
CE2->TC	++	1.43			ns
	--	1.21			ns
i = 0,1,2,3					
Tsu (SRN)		6.50			ns
Th (SRN)		0.00			ns
Tsu (PEN)		6.40			ns
Th (PEN)		0.00			ns
Tsu (CE1)		6.20			ns
Th (CE1)		0.00			ns
Tsu (Di)		2.35			ns
Th (Di)		0.00			ns
i=0,1,2,3					
PW (CLK)		1.95	3.80	3.02	ns
FAN-OUT LOAD LIMIT:		30			loads
k-FACTOR	RISING Qi	0.025			ns/LU
	FALLING	0.025			ns/LU
	RISING TC	0.030			ns/LU
	FALLING	0.025			ns/LU
MAXIMUM FREQUENCY OF OPERATION (fMAX)			56	70	MHz

---

* CLK, CE2 COUNT AS 2 LOADS EACH



ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

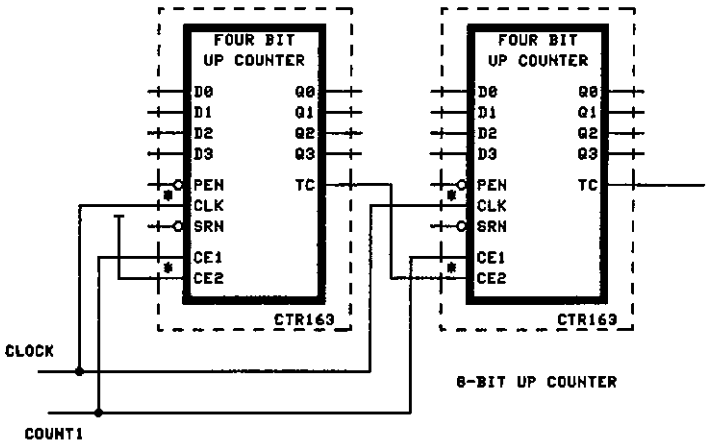
CTR163 14 B cells 4-BIT CNTR; SR

CTR163 is synchronously presettable for applications such as programmable dividers. The LOW-active preset enable input (PEN) allows presettable parallel loading of this counter with the contents of the data inputs (D0-D3) on the next rising edge of the clock (CLK). This macro provides two types of count enable inputs (CE1, CE2), and generates the terminal count indicator (TC) to allow versatility in multi-stage synchronous counting. TC signals the following stage to advance on the next clock. Either CE1 or CE2 will stop the counter from counting when disabled. CE2 will also force TC to zero. CTR13 has a synchronous reset input (SRN) that overrides counting and parallel loading and allows the outputs (Q0-Q3, TC) to be simultaneously reset on the rising edge of the next clock input.

FUNCTION TABLE

INPUTS						OUTPUTS
RESET SRN	LOAD PEN	ENABLE CE1	CE2	CLOCK CLK	Qi	TC
0	X	X	X	R	RESET Qi=0	0
1	0	X	1	R	LOAD	If sum Qi=15, TC=1 else TC=0
1	0	X	0	R	LOAD	0
1	1	0	1	X	STOP	If sum Qi=15, TC=1 else TC=0
1	1	X	0	X	STOP	0
1	1	1	1	R	COUNT UP	If sum Qi=15, TC=1 else TC=0
1	1	1	1	F	NO CHANGE	If sum Qi=15, TC=1 else TC=0

TC = Q3.Q2.Q1.Q0.CE2 . = AND
X = DON'T CARE
R = RISING EDGE
F = FALLING EDGE


FOUR BIT
UP COUNTER
D0
D1
D2
D3
PEN
CLK
SRN
CE1
CE2
Q0
Q1
Q2
Q3
TC
CTR163
FOUR BIT
UP COUNTER
D0
D1
D2
D3
PEN
CLK
SRN
CE1
CE2
Q0
Q1
Q2
Q3
TC
CTR163
CLOCK
COUNT1
6-BIT UP COUNTER

ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

DEC138 6 B cells 3:8 DECODER WITH HIGH ENABLE

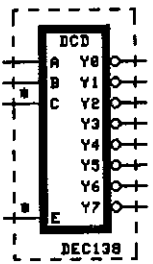
		S	
Tpd A,B,C->Yi+-		2.39	ns
	-+	1.48	ns
	E->Yi+-	2.15	ns
	-+	1.65	ns
i = 0,1,2,3,4,5,6,7			
FAN-OUT LOAD LIMIT:		30	loads
k-FACTOR	RISING ALL	0.025	ns/LU
	FALLING	0.025	ns/LU

---

* C, E COUNT AS 2 LOADS EACH
EACH OUTPUT HAS A FAN-OUT LIMIT OF 30

DEC138 has three select inputs (A, B, C), and provides eight mutually exclusive, active LOW outputs (Y0-Y7). The enable input (E) can be used to select input when expanding to a 4:16 line decoder.

E	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
0	X	X	X	1	1	1	1	1	1	1	1
1	0	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	0	1	1	1	1	1	1
1	0	1	0	1	1	0	1	1	1	1	1
1	0	1	1	1	1	1	0	1	1	1	1
1	1	0	0	1	1	1	1	0	1	1	1
1	1	0	1	1	1	1	1	1	0	1	1
1	1	1	0	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	1	0



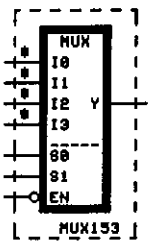
ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

MUX153 2 B cells 4:1 NON-INVRTNG. MUX WITH LO ENABLE

			S	
Tpd	EN->Y+-		0.47	ns
		-+	0.96	ns
	Ii->Y++		1.60	ns
		--	1.90	ns
	S0->Y++		2.57	ns
		+-	2.81	ns
		-+	2.91	ns
		--	3.10	ns
	S1->Y++		1.68	ns
		+-	1.41	ns
		-+	1.83	ns
		--	1.78	ns
i = 0,1,2,3				
FAN-OUT LOAD LIMIT:		Y	30	loads
k-FACTOR	RISING	Y	0.030	ns/LU
	FALLING		0.025	ns/LU

---

* Ii INPUTS COUNT AS 2 LOADS EACH



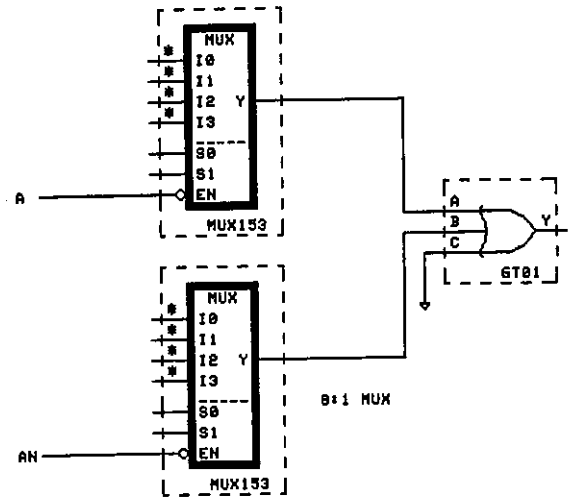
ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

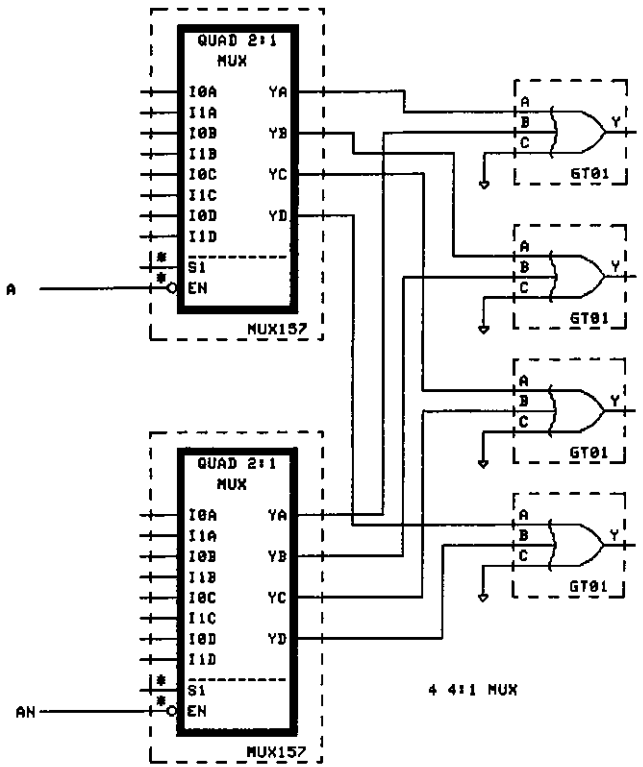
MUX153 2 B cells 4:1 NON-INVRTNG. MUX WITH LO ENABLE

MUX153 selects one data input from four sources (I0-I3). Output (Y) presents the selected data in its true form. MUX153 can also be used to generate 2-stage AND-OR functions of three variables. The active-low enable input (EN) can be used as a select input when expanding to a larger multiplexor (8:1, 16:1, ... 64:1). The outputs of two or more MUX153s are ORed together for a large multiplexor.

$$Y = I0.\overline{S0}.\overline{S1}.\overline{EN} + I1.S0.\overline{S1}.\overline{EN} + I2.\overline{S0}.S1.\overline{EN} + I3.S0.S1.\overline{EN}$$

EN	S0	S1	I0	I1	I2	I3	Y
1	X	X	X	X	X	X	0
0	0	0	0	X	X	X	0
0	0	0	1	X	X	X	1
0	1	0	X	0	X	X	0
0	1	0	X	1	X	X	1
0	0	1	X	X	0	X	0
0	0	1	X	X	1	X	1
0	1	1	X	X	X	0	0
0	1	1	X	X	X	1	1
0	X	X	0	0	0	0	0
0	X	X	1	1	1	1	1
X	X	X	0	0	0	0	0
0	X	0	0	0	X	X	0
0	X	0	1	1	X	X	1
0	X	1	X	X	0	0	0
0	X	1	X	X	1	1	1
0	0	X	0	X	0	X	0
0	0	X	1	X	1	X	1
0	1	X	X	0	X	0	0
0	1	X	X	1	X	1	1


MUX
I0
I1
I2
I3
S0
S1
EN
Y
MUX153
A
AN
GT01
A
B
C
Y
8:1 MUX


QUAD 2:1
MUX
I0A
I1A
I0B
I1B
I0C
I1C
I0D
I1D
S1
EN
YA
YB
YC
YD
MUX157
A
AN
GT01
A
B
C
Y
4 4:1 MUX

ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

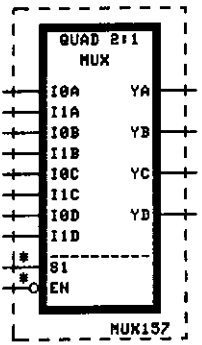
MUX157 4 B cells QUAD 2 TO 1 MUX WITH ENABLE LOW

		S	
Tpd I0i->Yi	++	1.40	ns
	--	1.70	ns
I1i->Yi	++	1.40	ns
	--	1.70	ns
S1->Yi	++	2.07	ns
	--	2.01	ns
EN->Yi	+-	0.46	ns
	-+	0.93	ns

i=A,B,C,D

FAN-OUT LOAD LIMIT:		30	loads
k-FACTOR	RISING	0.030	ns/LU
	FALLING	0.025	ns/LU

* S1 COUNT AS 2 LOADS
* EN COUNTS AS 4 LOADS



ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

MUX157 4 B cells QUAD 2 TO 1 MUX WITH ENABLE LOW

The MUX157 is composed of 4 2:1 MUXs, each of which selects one data input from two sources (I0i,Ili). The select input (SI) and the enable input (EN) are common to all the multiplexors. The outputs (Yi) present the selected data in true form. MUX157 can also generate 2-stage AND-OR functions of two variables. The active LOW enable can be used as a select input when expanding to a quad of larger multiplexors (four 4:1, four 8:1, etc.). The corresponding outputs of two or more MUX153s are ORed together for a large multiplexor.

i = A, B, C, D

EN	Sl	I0i	Ili	Yi
1	X	X	X	0
0	0	0	X	0
0	0	1	X	1
0	1	X	0	0
0	1	X	1	1
0	X	0	0	0
0	X	1	1	1
X	X	0	0	0

ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

REG164 16 B cells 8-BIT SR/PR SHIFT REGISTER W/RESET

		S TYP	MIL	COM	
Tpd CLK->Qi	++	2.65			ns
	+-	3.28			ns
ARN->Qi	--	2.61			ns
i= 1,2,3,4,5,6,7,8					
Tsu (A,B)		2.50			ns
Thd (A,B)		0.00			ns
Trec(ARN)		0.70			ns
PW (ARN)		2.78			ns
PW (CLK)		3.80	7.41	5.89	ns
FAN-OUT LOAD LIMIT:		30			loads
k-FACTOR	RISING	0.025			ns/LU
	FALLING	0.025			ns/LU
MAXIMUM FREQUENCY OF OPERATION (fMAX)			66	83	MHz

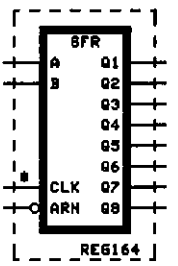
---

* CLK COUNTS AS 2 LOADS

REG164 is an 8-bit serial-in, parallel-out shift register. Serial data input (A,B) are synchronously entered through a 2-input AND gate on the rising edge of the clock input (CLK). The active-LOW reset input (ARN) clears this shift register asynchronously and sets all outputs (Q1-Q8) LOW independent of the clock.

ARN	CLK	A	B	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	
0	X	X	X	0	0	0	0	0	0	0	0	RESET
1	0	X	X	Q1n	Q2n	Q3n	Q4n	Q5n	Q6n	Q7n	Q8n	HOLD
1	R	1	1	1	Q1n	Q2n	Q3n	Q4n	Q5n	Q6n	Q7n	SHIFT IN 1
1	R	X	0	0	Q1n	Q2n	Q3n	Q4n	Q5n	Q6n	Q7n	SHIFT IN 0
1	R	0	X	0	Q1n	Q2n	Q3n	Q4n	Q5n	Q6n	Q7n	SHIFT IN 0

Qin = last steady state value



ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

REG175 9 B cells 4-BIT REGISTER WITH ASYNC. RESET

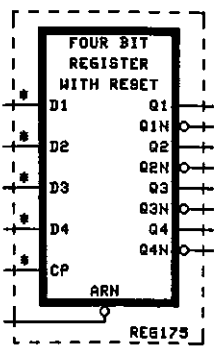
		S TYP	MIL	COM	
Tpd CP->Qi	++	1.97			ns
	+-	1.96			ns
CP->QiN	++	2.73			ns
	+-	2.14			ns
ARN->Qi	--	3.44			ns
ARN->QiN	-+	3.59			ns
i=1,2,3,4					
Tsu (D1,D2,D3,D4)		1.00			ns
Thd (D1,D2,D3,D4)		0.50			ns
Trec (ARN)		3.10			ns
PW (ARN)		2.64			ns
PW (CP)		1.95	3.80	3.02	ns
FAN-OUT LOAD LIMIT:		30			loads
k-FACTOR RISING		0.025			ns/LU
FALLING		0.025			ns/LU
MAXIMUM FREQUENCY OF OPERATION (fMAX)			130	165	MHz

* CP, D1, D2, D3, D4 COUNT AS 2 LOADS EACH

REG175 contains four flip/flops with a single data input each (Di). The clock input (CP) and reset input (ARN) are shared by all four flip/flops on the REG175. Both true and complemented outputs are provided for each flip/flop (Qi, QiN).

CP	Di	ARN	Qin+1	QiNn+1
X	X	0	0	1
R	0	1	0	1
R	1	1	1	0
0	X	1	Qin	QiNn

i = 1,2,3,4



ALL VALUES ARE TYPICAL AT VDD = 5.0V
TA = 25oC

REG373 7 B cells OCTAL D-LATCH TRANSPARENT HIGH

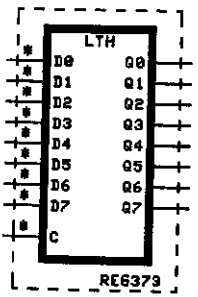
		S TYP	MIL	COM	
Tpd Di->Qi	++	0.96			ns
	--	1.33			ns
C->Qi	++	2.02			ns
	+-	2.58			ns
Tsu (Di)		0.00			ns
Th (Di)		1.50			ns
PW (C)		1.95	3.80	3.02	ns
i=0,1,2,3,4,5,6,7					
FAN-OUT LOAD LIMIT:		30			loads
k-FACTOR	RISING Q0->Q7	0.025			ns/LU
	FALLING	0.025			ns/LU
MAXIMUM FREQUENCY OF OPERATION (fMAX)			130	165	MHz

* ALL INPUTS COUNT AS 2 LOADS EACH

REG373 consists of eight D-type latches with a common clock. When the clock input (C) is HIGH, the latches are all transparent to the data inputs (Di). When the clock is LOW, the data inputs that meet the set-up time requirement are latched. The output (Qi) is available in true form only.

C	Qi
0	LATCHED
1	TRANSPARENT (Di)

i = 0,1,2,3,4,5,6,7



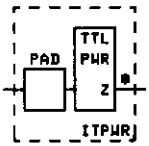
Section 6-6:

Special

ITPWR I/O CELL EXTRA VCC (+5V) PIN

REQUIRED WHEN AN ADDED TTL POWER PIN IS NEEDED.
USES THE PAD PORTION OF THE I/O CELL.
USED TO OBTAIN A CORRECT POPULATION REPORT AND EXTERNAL PIN COUNT BY THE AMCC MACROMATRIX ERC SOFTWARE.

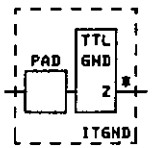
- GROUND THE INPUT PIN WITH THE WIRE POINTING UP
- TERMINATE THE OUTPUT

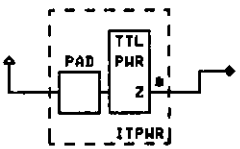


ITGND I/O CELL EXTRA TTL GND PIN

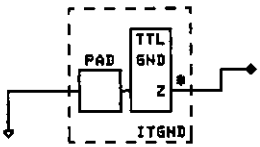
REQUIRED WHEN AN ADDED TTL GROUND PIN IS NEEDED.
USES THE PAD PORTION OF THE I/O CELL.
USED TO OBTAIN A CORRECT POPULATION REPORT AND EXTERNAL PIN COUNT BY THE AMCC MACROMATRIX ERC SOFTWARE.

- GROUND THE INPUT PIN WITH THE WIRE POINTING DOWN
- TERMINATE THE OUTPUT





PWRT00

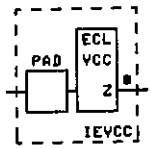


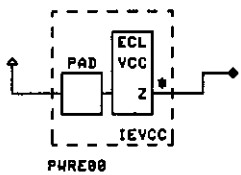
GNDT00

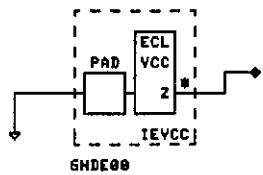
IEVCC I/O CELL EXTRA ECL VCC PIN

REQUIRED WHEN AN ADDED ECL VCC PIN IS NEEDED.
USES THE PAD PORTION OF THE I/O CELL.
USED TO OBTAIN A CORRECT POPULATION REPORT AND EXTERNAL PIN COUNT BY THE AMCC MACROMATRIX ERC SOFTWARE.

- GROUND THE INPUT PIN WITH THE WIRE POINTING DOWN
- TERMINATE THE OUTPUT







CHIP MACROS:

The chip macro documents the number of fixed power and ground pins that a particular array has for a given I/O mode. It also documents the internal pin count limit, the number of each type of cell available on a given array, the allowed cell utilization, the default power supply or supplies, the worst-case current multiplier for MIL and for COM product grades and other data as required by the AMCC MacroMatrix software.

- MUST BE USED - THE MACROMATRIX ERC SOFTWARE REQUIRES THAT A CHIP MACRO BE USED ON THE SCHEMATICS
- Follow directions in the MACROMATRIX USER'S GUIDE (Volume II, Section 8) and MACROMATRIX INSTALLATION MANUAL (Volume II, Section 7) to attach parameters or values to the chip macros AS REQUIRED
- Ground and terminate inputs and outputs as shown in the examples. The inputs to a chip macro are always tied to global ground regardless of the individual chip technology (BiCMOS, Bipolar).

Chip Macro Parameters:

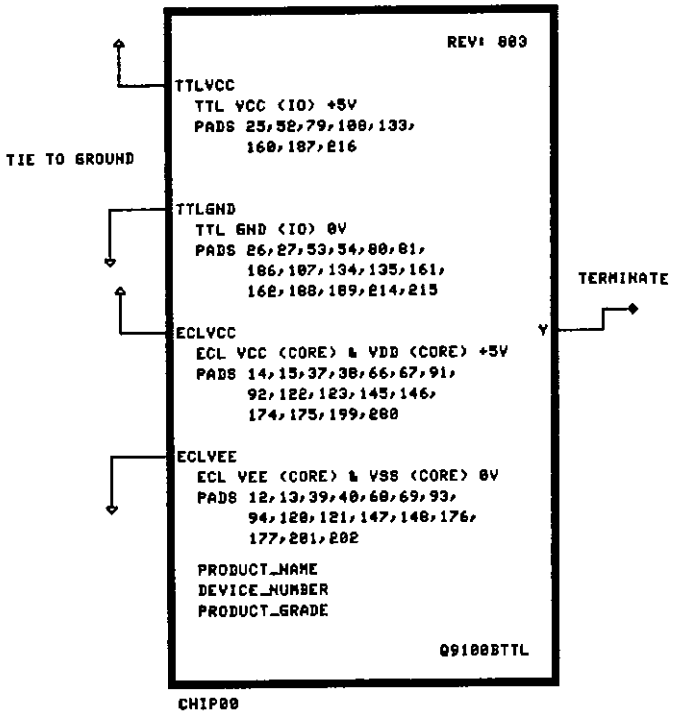
		TTL	100% ECL	MIX	+5MIX
PRODUCT_NAME	AMCC ASSIGNED NAME	X	X	X	X
DEVICE_NUMBER	AMCC ASSIGNED NUMBER	X	X	X	X
PRODUCT_GRADE	MIL OR COM	X	X	X	X
POWER_SUPPLY	FOR OTHER THAN DEFAULT	-	X	X	-

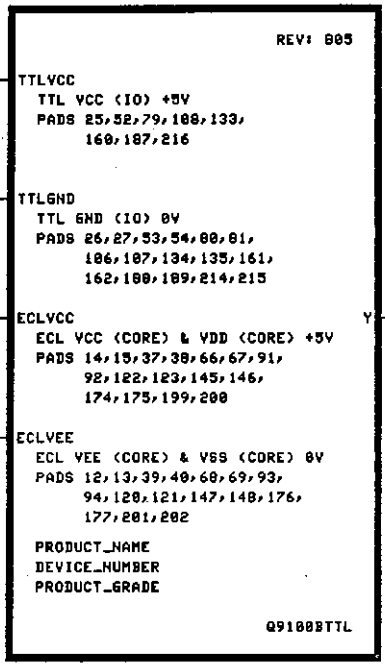
ALLOWED POWER_SUPPLY PARAMETER VALUES:

default	What appears on the chip macro graphic
STD4	-4.5V ECL VEE SUPPLY; ECL VCC = 0V
STD5	-5.2V ECL VEE SUPPLY; ECL VCC = 0V
5VREF	+5V ECL VCC SUPPLY; ECL VEE = 0V

FOR SINGLE POWER SUPPLY +5V CIRCUITS; 100% TTL

Q9100BTTL	FOR 100% TTL CIRCUIT ON A Q9100B
Q2100BTTL	FOR 100% TTL CIRCUIT ON A Q2100B





SAMPLE

CHIP MACRO

REVISION NUMBER HAS BEEN UPDATED

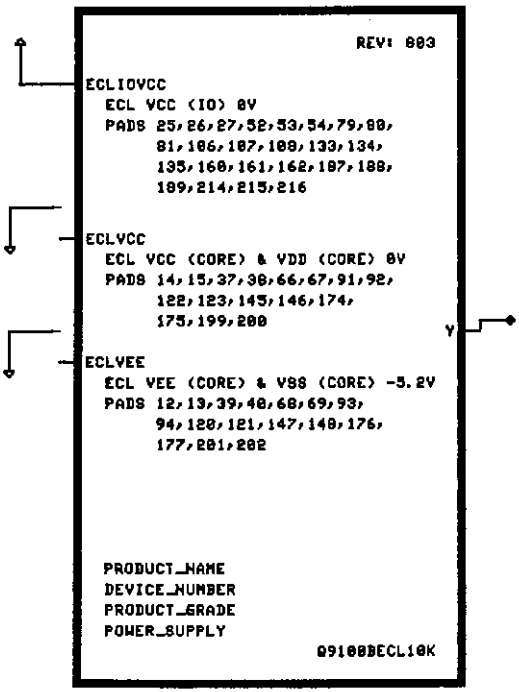
FOR SINGLE POWER SUPPLY -5.2V CIRCUITS; 100% ECL

ECL 10K INPUT:

Q9100BECL10K FOR 100% ECL 10K CIRCUIT ON A Q9100B
Q2100BECL10K FOR 100% ECL 10K CIRCUIT ON A Q2100B

ECL 100K INPUT:

Q9100BECL100K FOR 100% ECL 100K CIRCUIT ON A Q9100B
Q2100BECL100K FOR 100% ECL 100K CIRCUIT ON A Q2100B



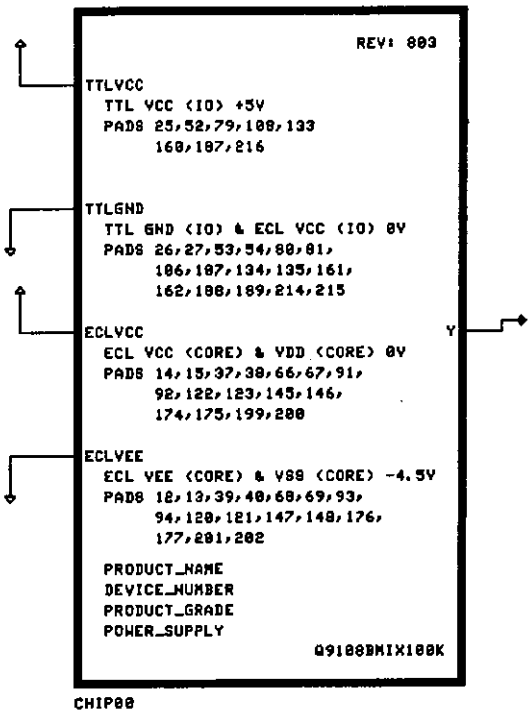
FOR DUAL POWER SUPPLY +5V; -5.2V CIRCUITS; ECL/TTL MIX

ECL 10K INPUT:

Q9100BMIX10K FOR ECL 10K/TTL CIRCUIT ON A Q9100B
Q2100BMIX10K FOR ECL 10K/TTL CIRCUIT ON A Q2100B

ECL 100K INPUT:

Q9100BMIX100K FOR ECL 100K/TTL CIRCUIT ON A Q9100B
Q2100BMIX100K FOR ECL 100K/TTL CIRCUIT ON A Q2100B



FOR SINGLE POWER SUPPLY +5V CIRCUITS; ECL/TTL MIX

ECL 10K INPUT:

Q9100BTTL10K FOR +5V REF ECL 10K/TTL CIRCUIT ON A Q9100B
Q2100BTTL10K FOR +5V REF ECL 10K/TTL CIRCUIT ON A Q2100B

ECL 100K INPUT:

Q9100BTTL100K FOR +5V REF ECL 100K/TTL CIRCUIT ON A Q9100B
Q2100BTTL100K FOR +5V REF ECL 100K/TTL CIRCUIT ON A Q2100B